0828.70005 PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re U.S. Patent Application)
)
Applicants: Yoshio Dejima)
)
Serial No.)
)
Filed: March 8, 2004)
)
For: THIN FILM TRANSISTOR)
SUBSTRATE AND METHOD FOR)
FABRICATING THE SAME)

I hereby certify that this paper is being deposited with the United States Postal Service as EXPRESS MAIL in an envelope addressed to: MS Patent Application, Commissioner for Patents, Alexandria, VA 22313-1450, on this date.

Mar. 8, 2004 *Express Mail No. EV032702583US*
Date

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This IDS is submitted under 37 C.F.R. §1.97(b) within either of the following time periods, whichever occurs last:

(a) within three months of either the filing date of the national application or the date of entry into the national stage; or

(b) before the mailing date of first office action on the merits (i.e., not including actions such as restriction requirements).

Applicant(s) submit herewith Form PTO-1449 (Information Disclosure Citation) together with copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 C.F.R. §1.56. Applicant(s) respectfully submit that the citation of any reference on Form PTO-1449 does not constitute an admission that the reference qualifies as prior art.

It is requested that the information disclosed on the enclosed Form PTO-1449 be made of record in this application.

The Commissioner is hereby authorized to charge any additional fees which may be required to this application under 37 C.F.R.§§1.16-1.17, or to credit any overpayment, to Deposit Account No. 07-2069. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 0828.70005	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT Yoshio Dejima		
	FILING DATE 3/8/2004	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	6,468,840	10/22/2002	Tanaka et al.	
	1B				
	1C				
	1D				
	1E				
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L	2001-311965	11/9/2001	Japan		partial
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	
	1R	
	1S	

EXAMINER	DATE CONSIDERED

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-311965
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(51)Int.Cl. G02F 1/1368
G09F 9/00
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H01L 29/786
H01L 21/336

(21)Application number : 2000-129820
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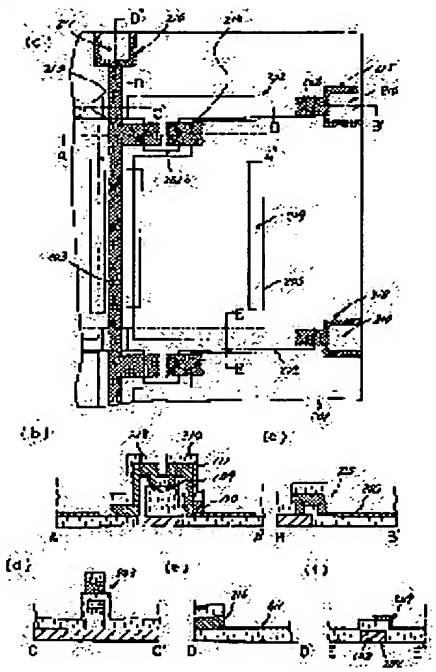
(71)Applicant : NEC CORP
NEC KAGOSHIMA LTD
(72)Inventor : TANAKA HIROAKI
UCHIDA HIROYUKI

(54) ACTIVE MATRIX SUBSTRATE AND MANUFACTURING METHOD THEREFOR

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a relay field system liquid crystal display device and a manufacturing method therefore realizing a low cost by reducing the number of production processes to three times PR processes.
SOLUTION: A gate island where gate electrodes, islands 201b, and pixel electrodes are formed on a transparent insulating substrate 101 is provided with laminated gate electrodes 102, a gate insulating film, and a semiconductor film, and further each film is formed in a plane form of the same size as or smaller than the gate electrode 102 and is coated with a channel protection film. By using a half-tone exposing method, it is possible to form a gate bus line 202 and the gate electrode, and the island 201b can be formed in the same PR process, and an opening part of the channel protection film and the pixel electrodes 209 can be formed in the same PR process, and the manufacture can be realized by the three times processes. Moreover, the side face of the island 201b can be coated with the channel protection film, and this prevents impurities from entering the semiconductor film by diffusion and an electric field and improves a characteristic of the TFT.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

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[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]